ASPIICS CCB: The Functional Control Electronics of an Externally Occulted Solar Coronagraph Instrument for the ESA PROBA-3 Mission

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Abstract: *PROBA-3 is a technology mission of the European Space Agency (ESA), devoted to the in-orbit demonstration of formation flying techniques and technologies. Presently at the end of phase B, PROBA-3 will implement a coronagraph (called ASPIICS, "Association de Satellites Pour l'Imagerie et l'Interferometrie de la Couronne Solaire") that will both demonstrate and exploit the capabilities and performance of formation flying. The ASPIICS Coronagraph Control Box (CCB) which has the central role and controls all the activities of the coronagraph instrument sub-systems while being the only I/F with the spacecraft, is composed of the Coronagraph Control Module (CCM) which is in charge of the command and control of the entire instrument, of the image data compression unit and of the interface with the spacecraft, the Power Converter Module (PCM) which provides the power to all modules of the CCB, the Motor Control Module (MCM) which controls and commands all motors inside the Coronagraph Optical Box (COB), and the Ancillary Electronics Module (AEM) which is in charge of the Shadow Position Sensor (SPS) data acquisition and treatment and of the active thermal control. In this paper after a brief overview of the PROBA-3 ASPIICS coronagraph, the typical observation sequences and derived requirements, a detailed description of the architectural definition of the ASPIICS Coronagraph Control Box (CCB) electronics at the Preliminary Design Review (PDR) status, is provided.*

Keywords: *PROBA-3, ASPIICS, Coronagraph Control Box, Data Processing Unit*

1. Introduction and general architecture of the ASPIICS coronagraph

PROBA-3, the 3rd mission of the ESA PROBA (PRoject for On-Board Autonomy) series, is an experimental mission under the Element 4 of the ESA General Support Technology Programme (GSTP); it is devoted to the demonstration of technologies and techniques for highly-precise satellite formation flying in the context of a large-scale solar science experiment. Its space segment is composed of two satellites, derived from ESA's standard PROBA platform that will be launched together into a highly elliptical orbit around the Earth.

The two satellites compose a giant (≈ 140m) externally-occulted Solar Coronagraph System, (called ASPIICS coronagraph, termed from "Association de Satellites Pour l'Imagerie et l'Interferometrie de la Couronne Solaire") with one of them carrying a Sun-occulting disk (Occulter Spacecraft – OSC) and the other one carrying the coronagraph instrument with the associated optics, electronics and detectors (Coronagraph Spacecraft – CSC) for Solar coronal imaging. The coronagraph instrument itself is based on an axis-symmetrical diffractive optical system imaging the corona on a passively cooled CCD. The instrument also includes a front door mechanism for protection against dust and direct solar flux when it is not in formation flying, a shutter mechanism to ensure accurate exposure time and a filter wheel. The images will be acquired during the observation periods at the apogee of the orbit and stored on-board where they will be compressed afterwards before being down-linked to the ground. The instrument will observe the corona with wide band filter [540 nm – 570 nm], narrow band filter around He I D3 line at 587.6 nm and with different polarisations. This pioneering coronagraph system will perform high spatial resolution imaging of the solar corona from the coronal base (1.04 solar radii) out to 3 solar radii by creating an artificial solar eclipse in space.

It is expected to revolutionize solar coronal science by providing long duration observations of the inner corona with unprecedented spatial resolution and contrast (low stray light), surpassing the observations of the few minutes only duration a year solar eclipses available from the ground. Besides being a complex, realistic and ambitious science mission, the demanding requirements of the coronagraph system experiment make it a perfect payload instrument to demonstrate high precision formation flying.

The ASPIICS coronagraph instrument itself is composed of the Coronagraph Optical Box (COB), of the Camera Electronics Box (CEB) and of the Coronagraph Control Box (CCB). The coronagraph instrument is mounted on the Coronagraph Spacecraft (CSC) while the Occulter Disk is mounted on the Occulter Spacecraft (OSC). The COB holds the optics, the detector and its radiator, the Front Door Assembly (FDA), the Filter Wheel Assembly (FWA) and the Shutter Mechanism (SHM). The metrological sensors are the Shadow Position Sensor (SPS) and the Occulter Position Sensor Emitter (OPSE). The SPS is mounted in the COB and its operation is fully integrated in the COB operations. The OPSE (set of LEDs) is mounted in the centre of the Occulter Disk and is observed by the instrument.

The ASPIICS instrument is developed by a consortium of European Institutes and Industries from Belgium, Czech Republic, France, Germany, Greece, Italy, Luxembourg and Russia.

2. Typical observation sequences and requirements

Two observation periods are foreseen per week for the ASPIICS coronagraph instrument, each of 6 hours, and the allowed volume for telemetry leads to a possible data volume of 8 Gbits per period.

Four types of observation sequences have been defined, and give the constraints for the dimensioning of the system:

- The synoptic continuous imaging, which is the background sequence during the observation period. It consists of consecutive full 2Kx2K images with 16 bits dynamic range and cadence at 60 seconds.
- The polarimetric imaging, one sequence embedded every 0.5 hour in the main synoptic continuous imaging. This sequence includes one continuum image recorded before and one after the four polarisation images. The Polarimetric images are full 2Kx2K images with 16 bits dynamic range (i.e. 64 Mbits per image) and total cadence for all 6 images at 72 seconds.
- The Helium line imaging, one sequence embedded every 0.5 hour in the main synoptic continuous imaging. This sequence consists of 3 consecutive images and it is embedded every 0.5 hours in the main synoptic continuum imaging. The Helium line images are full 2Kx2K images with 16 bits dynamic range and total cadence for all images at 240 seconds (exposure time 75 seconds).
- The fast dynamical imaging sequence, which is necessary for the identification of waves. This sequence consists of consecutive 1Kx1K images (full frames with binning 2x2 implemented during readout or windows located in one of the four corners of the detector area) with 16 bits dynamic range and very strict cadence at 2 seconds.

The above sequences lead to the following possibilities of observation that satisfy the 8 Gbits telemetry limitation, assuming an overhead of 20 % for packetisation:

- 5.8 hours of synoptic continuous imaging (348 images) combined with 0.2 hours of polarimetric imaging (60 images) resulting in a total data volume of 7.65 Gbits with a compression ratio of 4.
- 5.3 hours of synoptic continuous imaging (320 images) combined with 0.7 hour of Helium line imaging (30 images) resulting in a total data volume of 6.56 Gbits with a compression ratio of 4.
- 3.5 hours of synoptic continuous imaging (210 images) combined with 1.4 hours of fast dynamical imaging (2520 images) resulting in a total data volume of 7.88 Gbits with a compression ratio of 8.
- 6 hours of fast dynamical imaging (10800 images) resulting in a total data volume of 25.31 Gbits with a compression ratio of 8.

The last one is the worst case scenario (and the best for science). Such scenario shall be exceptionally used, and when used such huge data volume should be compressed and stored in the instrument memory for several days. The strategy for downlink in this case is to send 1 compressed image out of 4 with compression factor 8 and to downlink part of the remaining compressed images only if an interesting event has been observed in the received samples or by others coronagraphs. Otherwise, the whole sequence is thrown away.

Two opposite detector outputs are used for readout and thus image data temporal storage in an internal mass memory and rearrangement is required before compression and sending to the S/C mass memory. Since the required power budget for concurrent data acquisition, rearrangement, compression and storage is not available, the image data compression and possibly rearrangement will be performed off-line after the end of the observation period of 6 hours.

From the above sequences, the fast dynamical imaging is the most constraining and gives dimensioning for data memory size and compressor performances:

- A Mass Memory of at least 256 Gbit shall be implemented at CCB.
- All images (at most 10800) will be compressed after the observation in 1 hour, to limit the consumption of electrical power, resulting in a HW implementation of the image data compressor that achieves a throughput of 3 Msamples/s.

3. Image Data Compression Selection

The ASPIICS on-board image data compressor will be based on the Consultative Committee for Space Data Systems (CCSDS) 122 Image Data Compression (IDC) algorithm [1]. This algorithm is suitable to compress gray-scale images with up to 16-bit dynamic range and provides the following benefits:

- Suitable for use on-board spacecraft (best trade-off between compression performance and complexity, high-speed and low-power hardware implementation feasible, memory-efficient implementation).
- Lossless and high-quality lossy compression.
- Segment-based compression with segment size trade-off: data protection and memory size vs. compression effectiveness and rate-distortion performance.

The compression performance evaluation and the detailed quality analysis of the IDC algorithm was based on specific images (the eclipse image POISE and space images from LASCO C1). It concludes that CCSDS 122 (with segment size S=256 or 128) provides lossless and high fidelity lossy compression up to compression ratio 8 without requiring any preprocessing.

4. Dynamically reconfigurable payload data processing units

The advantages of the on-board radiation-tolerant dynamic reconfigurable payload data processing units (DPUs) that exploit partial/dynamic reconfigurability of SRAM-based FPGAs are summarized as follows:

- They provide system level advantages by supporting planned, mode-dependent functional alterations and unplanned updates, and mission operational advantages by allowing upgrades (due to changing of operational requirements, improvement of image and data processing algorithms and in response to in-flight calibration or single event effects (SEE) mitigation) after launch that enhance mission profile and thus extend valuable system life time.
- They provide in-flight dynamic adaptability with time-space partitioning of on-board data processing cores.

Therefore, an in-flight dynamically reconfigurable space grade FPGA is the most suitable solution to be in charge for image data compression also taking into consideration the results of the ESA study on a Dynamically Reconfigurable Processing Module (DRPM) [2].

The Xilinx rad-tolerant Virtex-4QV SX55 reconfigurable SRAM-based FPGA has been selected that provides high performance, high density and capability for CF1140 package assembly qualification. It is also used in the DPU of the Polarimetric and Helioseismic Imager instrument of ESA Solar Orbiter mission [2]. In this FPGA the internal configuration memory, routing resources, user flip-flops and BlockRAMs are susceptible to Single Event Upsets (SEUs). Therefore mitigation techniques like configuration memory scrubbing are applied. The Virtex-4 FPGA SelectMAP interface provides the most efficient, post-configuration read/write access to the configuration memory array. Triple Modular Redundancy (TMR) is not needed since on-board image data compression does not command/control any external interfaces and is not system critical. Logic isolation can be applied instead. SoCWire is designed to isolate any logic containing corrupted elements. Functional testing with test images for error detection targeting SEU and possible permanent faults shall be applied. Functional testing ensures the normal operation during system start-up, periodically and can distinguish permanent from transient faults.

5. Coronagraph Control Box structure

The Coronagraph Control Box (CCB) consists of a metallic box that houses five individual electronic modules and it has the central role controlling all the activities of the coronagraph instrument sub-systems while being the only I/F with the spacecraft, for commands, controls or data exchanges. More specifically the modules that are incorporated within the CCB are the following:

- The Coronagraph Control Module (CCM), which is in charge of the command and control of the entire instrument, of the image data compression unit and of the interface with the spacecraft.
- The Power Control Module (PCM), which provides the power to CCB modules.
- Filter Wheel & Front Door Module (FW_FD_M), which controls and commands the filter wheel and the front door inside the Coronagraph Optical Box (COB).
- Shutter Control Module (SCM), which controls and commands the shutter inside the Coronagraph Optical Box (COB).
- Ancillary Electronics Module (AEM), which is in charge of the Shadow Position Sensor (SPS) data acquisition and treatment and of the active thermal control.

A brief outline of the CCB can be reported as a closed box, housing 5 electronic PCB cards, which are mounted on separate metallic brackets (see Fig. 1). These modules are interconnected through a backplane unit which is designated as the motherboard module of the electronic system. The backplane is also supported to a metallic plate, designed in order to withstand the required operational and vibrations loads.

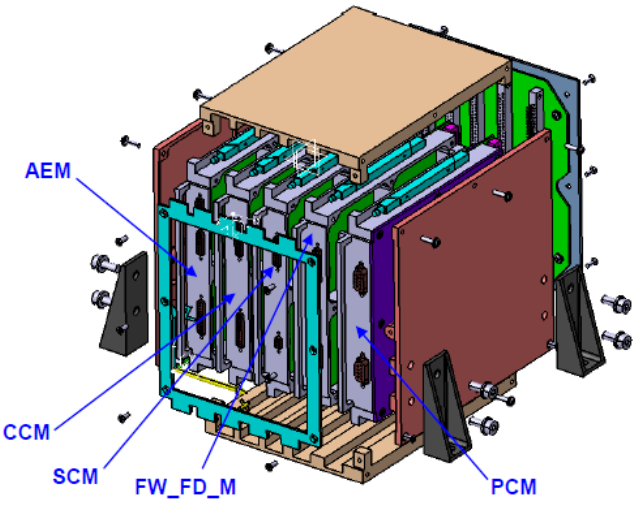

Figure 1: CCB Exploded View.

6. Coronagraph Control Box architectural definition

The block diagram of the ASPIICS coronagraph instrument electronics is shown in Fig. 2. Since there is only one Focal Plane Assembly (FPA) and Camera Electronics Box (CEB) and also only one interface to the S/C, all modules inside the CCB are not redundant at all. In Fig. 2 the Filter Wheel & Front Door Module (FW_FD_M) and the Shutter Control Module (SCM) constitute the Motor Control Module (MCM).

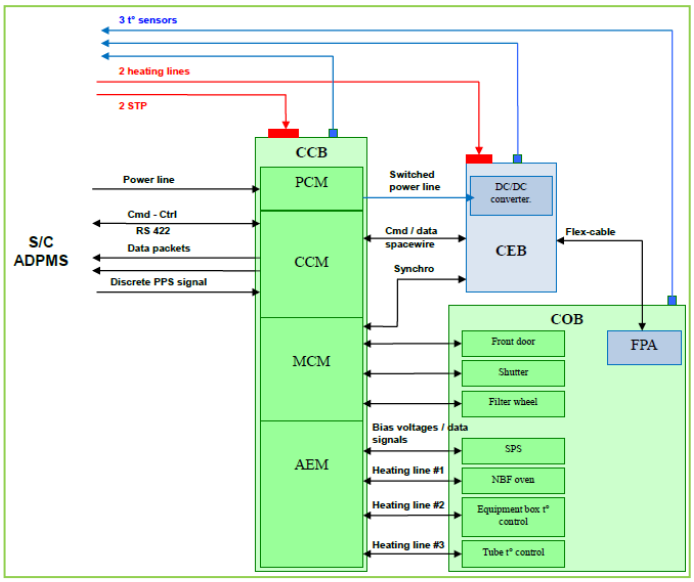

Figure 2: CCB block diagram.

7. Coronagraph Control Module (CCM)

The CCM is the heart of the entire ASPIICS instrument and is based on a flexible System-on-Chip (SoC) approach with heritage from DPUs in the Venus Monitoring Camera (VMC) and the Dawn Framing Camera. This has the advantage of maximal re-use of hardware and software modules and thus minimum risk in development, cost and schedule.

The CCM utilizes a combination of a LEON-3 based main processor system within a fixed, radiation hardened and triple modular redundancy (TMR) by design, one-time programmable fixed FPGA (Microsemi RTAX) together with a dedicated image data compression core implemented within a reconfigurable FPGA (Xilinx Virtex-4QV). Since image data compression is implemented in the reconfigurable FPGA, the only moderate processing power (20-30 MIPS) of the LEON-3 processor is sufficient for overall high-level instrument control and for communications with the S/C platform. All interfaces and instrument control/monitoring functions needed for basic operations are integrated in the fixed FPGA to achieve the highest reliability. Additionally, this FPGA acts as system supervisor to achieve the configuration control and the required configuration memory scrubbing for SEE radiation tolerance of the reconfigurable FPGA, supported by a high-reliable duplicated 512 Mbit NOR flash memory for configuration storage. The ASPIICS instrument software (for on-board processing and adaptability, autonomous safe control and monitoring, and data acquisition, storage and packetization, etc.) is stored in the same high-reliable duplicated 512 Mbit NOR flash memory.

The limited telemetry rate combined with the large science data volume demands sophisticated on-board image data compression. This is achieved by dedicated, in-flight reconfigurable processing cores attached to the running system by a flexible and glitch-free on-chip communication architecture, named System-on-Chip Wire (SoCWire). SoCWire is based on the well established ESA SpaceWire interface standard. Such a reconfigurable system is currently developed at IDA in the frame of the ESA Dynamically Reconfigurable Processing Module (DRPM) study [2].

On-board image data compression will be implemented in hardware (as an accelerator) to fulfill the real-time processing requirements. The CCSDS IDC algorithm has been adopted for HW implementation. HW implementation provides high performance allowing about two orders of magnitude less data processing execution time than the corresponding SW one. The CCSDS IDC algorithm will be implemented in the Xilinx rad-tolerant Virtex-4 QV SX-55 FPGA.

A complete non-volatile reliable mass memory (NAND flash memory) providing significant storage capacity fulfills all needs of intermediate data storage at very low resources need. An anticipated memory capacity of 256 Gbit is more than sufficient and leaves ample capacity for future changes. For high data rates, it is directly controlled by a DMA-type of flash memory controller within the RTAX FPGA. The design of the NAND-Flash memory will have complete error correction, taking into account the Flash handling. NAND Flash based mass storages for space applications have been intensively studied by IDA in the ESA Safe Guard Data Recorder (SGDR) study and are developed for the Sentinel-2 SSMM.

The hardware components of the CCM (see Fig. 3) are the following:

- The rad-hard Microsemi RTAX2000 FPGA with LEON-3 processor core, NAND-flash memory controller and interfaces to S/C and all equipment (PCM, MCM, AEM), including triple modular redundancy (TMR).
- The rad-tolerant Xilinx Virtex-4 FPGA with an image data compression core.
- The duplicated 512 Mbit non-volatile NOR flash memory for program and configuration storage, with error correction mechanism.
- The 256 Gbit non-volatile NAND flash mass memory for data storage, including dedicated error correction mechanism.
- The 2 Gbit SDRAM memory for processor program and data, with error correction mechanism.
- Additional components like bidirectional drivers, LVDS drivers/receivers, an RS-422 driver/receiver, an internal crystal oscillator, and power switches for Virtex FPGA and non-volatile memories.

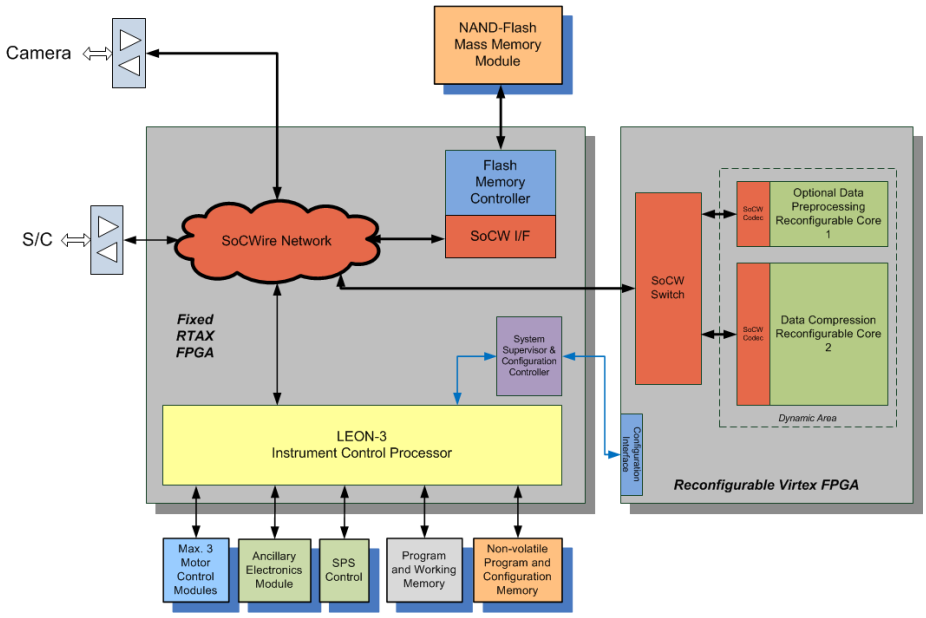

Figure 3: CCM architecture.

The ASPIICS instrument on-board software integrated in the CCM (and run by the LEON-3 processor core) carries out the following functions:

- It receives and maintains the ASPIICS instrument time which is synchronized to the S/C time via the PPS signal.
- It communicates with the S/C with a serial RS-422 command/control/status interface.
- It commands/controls the operation of camera electronics via a SpaceWire interface.
- It receives the science image data (16-bit pixels) via the SpaceWire interface from the Coronagraph Electronics Box (CEB) and, then, it stores (writes) this data in the mass memory (with rearrangement done in working data memory).
- It reads the science image data from the mass memory and sends them through a SoCWire interface at the reconfigurable FPGA for image data compression.
- It receives back the compressed science image data through a SoCWire interface, and then it adds time and formats in data packets to send via a PacketWire LVDS interface to S/C. Two PacketWire LVDS I/Fs are available for writing compressed science data to two S/C mass memory modules, respectively.
- It controls (on-off) the switches for CEB power control and motor drivers control, respectively, of the PCM via two serial UART LVDS interfaces.
- It receives from the PCM the status of DC-DC converters via a serial UART LVDS interface.
- It commands/controls and synchronizes the operation of motor mechanisms of shutter, front door and filter wheels, as well as, the redundant front door pin puller via a serial UART LVDS interface.
- It receives from the MCM, the shutter position data (produced by two independent mechanisms, that is, an optical encoder and a magnetoresistive sensor), the front door position data and the filter wheel position data via a serial UART LVDS interface.
- It commands/controls and synchronizes the operation of Shadow Position Sensor (SPS) signal processing and the thermal control via a serial UART LVDS interface.
- It receives, from the AEM part dedicated to SPS acquisition, the digitized SPS signals (4 samples of 8 sensor values with an update rate of 10Hz) and a sun alarm via a serial UART LVDS interface.
- It extracts from the digitized SPS signals the position of the umbra with respect to the centre of the pupil diaphragm and then it adds time and formats in data packets to send via a serial RS-422 interface to S/C. To do this the CCM must receive the ISD value from S/C.
- It receives, from the AEM part dedicated to temperature control, the thermal sensor data via a serial UART LVDS interface.
- For all HK data, it adds time and formats in data packets to send via a serial RS-422 interface to S/C.

Since all data processing steps are performed by a dedicated reconfigurable FPGA, the only moderate processing power (20-30 MIPS) of the LEON-3 processor is sufficient for overall high-level instrument control and for communications with the S/C platform.

8. CCSDS 122 Image Data Compressor (IDC)

The CCSDS-IDC algorithm [1] consists of two functional parts: a) a Discrete Wavelet Transform (DWT) unit that performs decorrelation and b) a Bit Plane Encoder (BPE) unit which encodes the decorrelated data. To limit the effects of data loss that may occur on the communications channel, the DWT data are partitioned into segments, each loosely corresponding to a different region of the image. Each segment is compressed independently, so that the effects of data loss or corruption are limited to the affected segment. Partitioning the DWT data into segments has also the benefit of limiting the memory required. The segment size can be adjusted to trade the degree of data protection and memory requirements for compression effectiveness and rate-distortion performance; smaller segments provide increased protection against data loss and low memory requirements, but tend to reduce the overall compression ratio and reconstructed image quality for lossy compression.

The CCSDS-IDC algorithm is implemented in hardware as an IP core in the reconfigurable Virtex-4QV SX55 FPGA. The CCSDS-IDC core architecture provides a powerful, cost-effective and highly integrated solution since it does not require any external memory (no extra memory interface, cost, mass and power overhead). The characteristics of the CCSDS-IDC IP core architecture are summarized as follows:

- Single-chip FPGA solution with efficient use of FPGA embedded memory based on a memory efficient DWT architecture.
- Early bit-depth calculation alleviating part of the BPE throughput bottleneck.
- High data-rate performance by using of pipelined data flows and exploiting algorithm inherent parallelism targeting the BPE bottleneck.
- High lossy compression quality exploiting large values of segment size.

Pipelined data flows include a) pipelining through FIFO queues, b) pipelining the three levels of 2-d single-level DWT c) pipelining key BPE processing steps (block scanning for AC coefficient binary word generation, mapping AC coefficient binary word to symbols and entropy encoding of mapped symbols). Algorithm inherent parallelism exploitation targeting the BPE bottleneck includes a) parallel implementation of segment header coding, initial (Rice) coding of quantized DC coefficients, Rice coding of BitDepthAC_Block$_m$ values and bit-plane encoding, b) parallel implementation of entropy encoding of mapped symbols for parents, children and grandchildren and c) block-level parallelism where multiple block-level processing in implemented in parallel along with efficient code option selection for a gaggle (16-blocks). It should be noted that the implemented parallelism is limited by the available FPGA resources.

The top level architecture of the implementation of CCSDS-IDC consists of three main units (see Fig. 4): a) DWT, b) Segment Buffer & Bit Depth Calculation c) BPE along with a Controller unit which, besides being the main CCSDS-IDC core controller, it also implements the configuration registers available for CCSDC-IDC configuration and control.

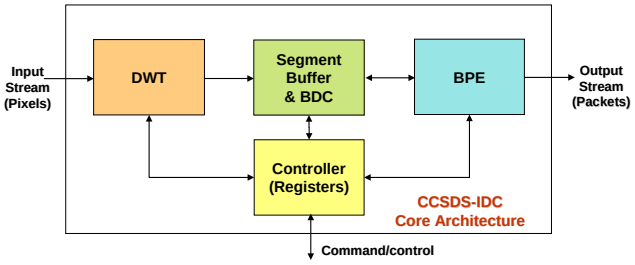

Figure 4: CCSDS-IDC top level architecture.

Discrete Wavelet Transform (DWT)

The DWT unit performs the decorrelation of the input pixels in order to provide the BPE with coefficients organized into subbands and blocks. In the proposed architecture (Fig. 5), the DWT implements the non-linear, integer approximation to a 9/7 DWT which is simply referred to as “Integer DWT”. Since the Integer DWT requires only integer arithmetic, it is capable of providing a) lossless compression which is imposed by the mission requirements and b) low implementation complexity which has a direct positive impact on power dissipation.

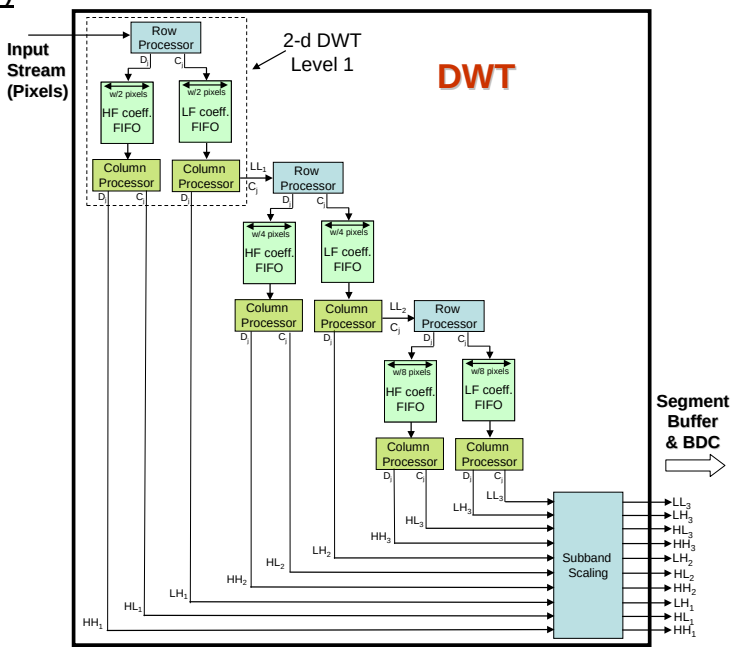

Figure 5: DWT architecture.

Segment Buffer & Bit Depth Calculator (SB&BDC)

The Segment Buffer & BDC unit (see Fig. 6):

- performs early bit-depth calculation thus alleviates part of the BPE throughput bottleneck (BPE does not have to access a whole segment of coefficients to perform bit depth calculations before starting bit plane encoding),
- implements the segment DWT coefficients buffer,
- provides BPE with the capability of sequential access to all (S) blocks in the segment in the required raster scan order,
- provides BPE with high-performance, parallel, block level access (BPE can fetch 1 block in just 4 BRAM read accesses).

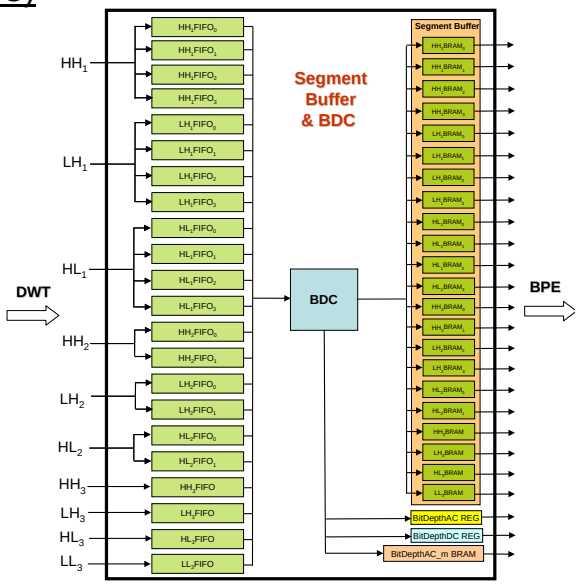

Figure 6: SB&BDC architecture.

Bit Plane Encoder (BPE)

The BPE is the key part of CCSDS-IDC and it is considered as the bottleneck of throughput performance and FPGA resources. The BPE reads DWT decorrelated data from the Segment Buffer, encodes DWT coefficient data and places the encoded output in the compressed data stream. Bit plane encoding of DWT coefficients proceeds segment-by-segment and each segment is coded independently of the others. The proposed BPE architecture (Fig. 7) is a parallel, pipelined architecture, exploiting inherent parallelism of CCSDS-IDC BPE processing tasks and the high density and memory capacity of SRAM FPGAs to speed-up the image compression throughput while being within the limited power budget.

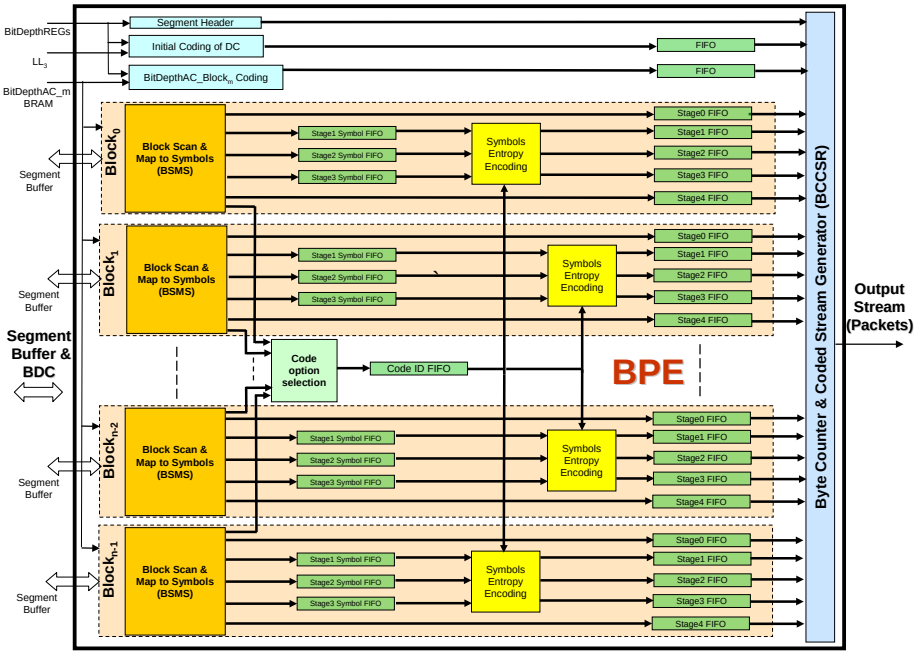

Figure 7: BPE architecture.

9. Power Control Module (PCM)

The CCB is the first equipment which is switched on after an OFF mode, by activating the only power line delivered by the S/C. This primary line powers the DC-DC converter inside the PCM, and in particular, the CCM, which, after the short time for boot and initialisation, is able to control the distribution of primary or secondary power to the others modules. A power distribution unit with DC-DC converters, regulators, filters and switches is effectively included inside the PCM, as shown in Fig. 8, which has to:

- power the Camera Electronics Box (CEB) by a switch-on of the primary power line for the CEB, under the control of the CCM,
- deliver the primary power to the Ancillary Electronics Module (AEM) to power the heaters needed for COB warming, thanks to the dedicated amplifiers,
- deliver the primary power to the MCM to power the pin puller inside the Front Door Assembly thanks to a dedicated switching system,
- power the MCM after a short time needed to initialise circuits of motor controllers in order to avoid the risk of motor jump at switch-on, under the control of the CCM.

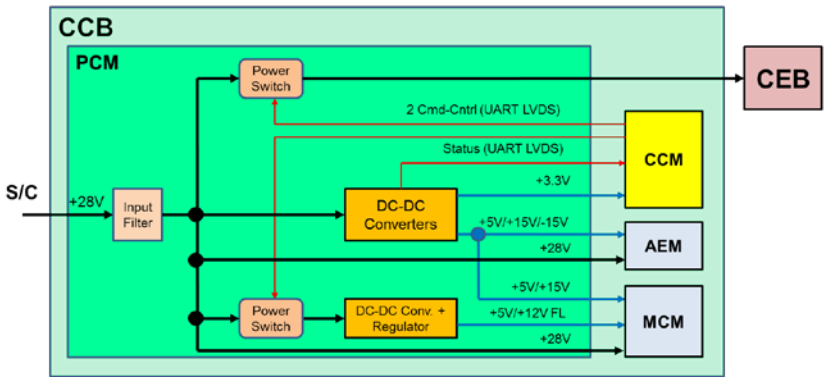

Figure 8: PCM architecture.

10. Motor Control Module (MCM)

The MCM, shown in Fig. 9, has to command and control the activities of all motors inside the Coronagraph Optical Box (COB):

- the Filter Wheel Assembly stepper motor,
- the Front Door Assembly main motor, which is a stepper motor, and a pin puller system able to open the door in case of failure of the main motor,
- the Shutter Mechanism, using a DC brushless, limited angle torque motor.

The MCM includes the motor drivers, the position sensors acquisition and conditioning electronics, and all circuits needed to control the position or speed loops. This module receives from the CCM all commands for mechanism activations, controls the motors accordingly, and sends back to the CCM the new positions reached by the mechanisms. Only one microcontroller is used for the 3 motor controls since the motors are not running at the same time. Physically, this sub-system is implemented on 2 boards in the CCB. The first board, termed Filter Wheel & Front Door Module (FW_FD_M), includes the microcontroller and the circuits needed for the 2 mechanisms using stepper motors, and the second one, termed Shutter Control Module (SCM), includes the electronics needed for the shutter mechanism control.

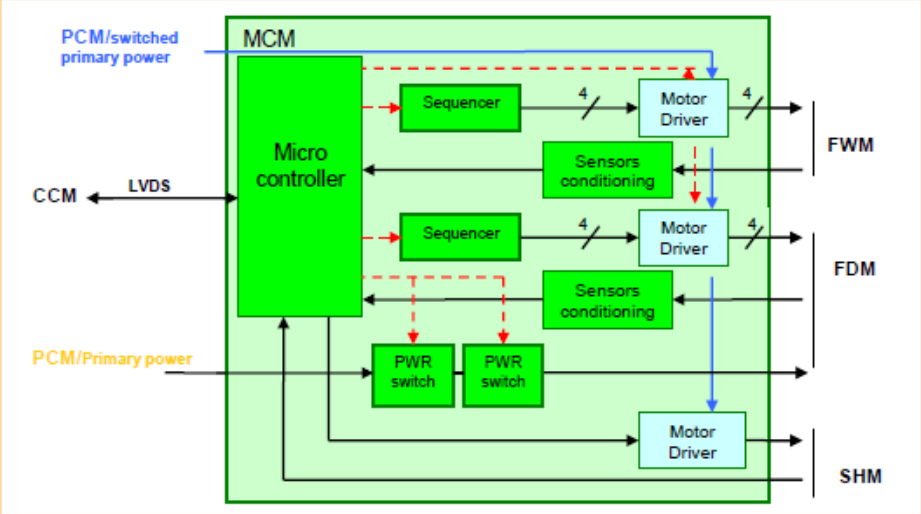

Figure 9: MCM architecture.

11. Auxiliary Electronics Module (AEM)

The AEM is responsible for the acquisition and treatment of the data delivered by the SPS head, before sending them to the CCM, and the temperature control of 2 controlled zones of the COB. The AEM also supplies the regulated voltages needed by the SPS head under the CCM control.

The first part of the AEM which is dedicated to the acquisition and treatment of the data delivered by the SPS head is shown in Fig. 10. This part of AEM receives from the SPS head 8 differential signals coming from the 8 light sensors and 2 temperature signals. It has to power the SPS head by a symmetrical power supply. The differential signals are received by instrumentation amplifiers, followed by two

double multiplexers authorizing the selection of two signals at a time out of eight received from the SPS head. These two signals are digitalized by two 16 bits ADC at a cadence of 40 samples/s, before delivering to the CCM for the estimation of the position of the umbra with respect to the centre of the pupil diaphragm. The temperature sensors needed by the SPS (2 in the head and 2 close to the ADC) are also conditioned by the AEM.

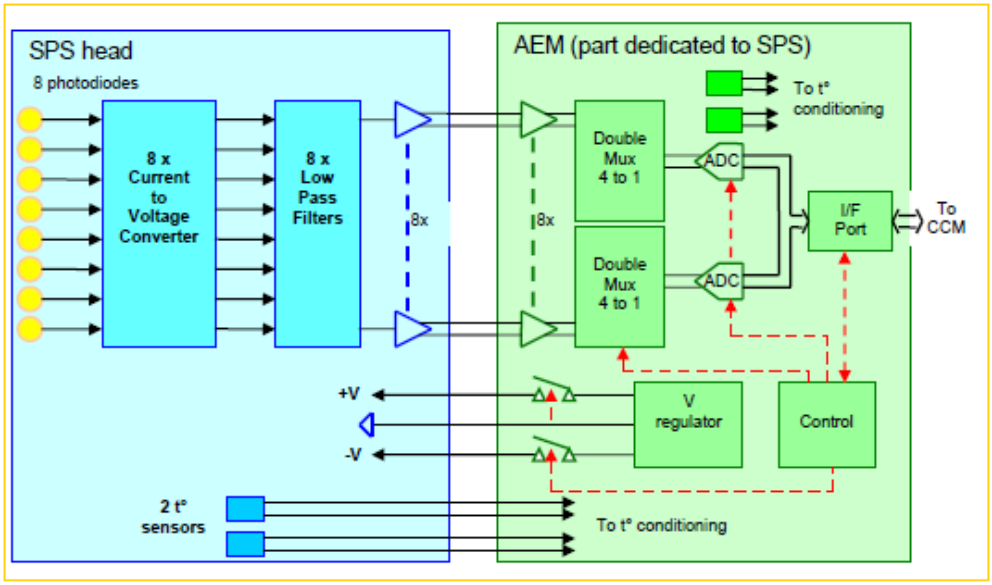

Figure 10: AEM architecture for SPS data acquisition.

The second part of the AEM which is dedicated to the temperature control of two zones (the front tube of the COB and the Equipment Box of the COB) is shown in Fig. 11. The temperature control of each zone is achieved by a comparison of the temperature order received from the CCM and the effective temperature measured in the zone. Two temperature values are received from the two temperature sensors mounted in the zone. Differences between these two temperatures (order and effective) are amplified in a PID controller and converted in a pulse width modulation at a fixed frequency of 20 Hz (controller and PWM are in software) and finally amplified to power the heaters of the zone. Two heaters and two power amplifiers are used for redundancy aspects. All temperature sensors are received by two multiplexers to avoid a single point of failure, amplified (2 amplifiers) and converted (2 ADCs) in digital on 12 bits.

The control circuit of the board has to:

- receive the temperature commands from the CCM, and deliver them to the three PID controllers,
- receive from the CCM the PID coefficients for the PID controllers,
- inhibit the use of power under control from the CCM, since only one motor is activated to avoid a too high power peak consumption,
- synchronize the acquisition of temperature values, by controlling the two multiplexers and the two ADCs,
- evaluate the median value of the three temperature sensors of each zone, before delivering to the PID controller,
- send to the CCM the values of the 11 temperature sensors.

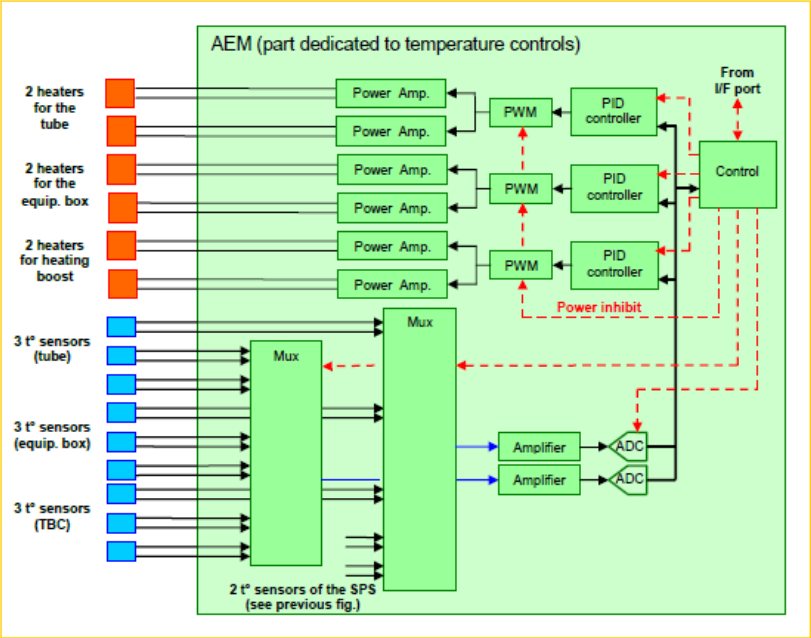

Figure 11: AEM architecture for thermal control.

12. Software architecture

The S/W of ASPIICS draws substantial heritage from instrumentation on earlier missions (SOHO-SUMER, ROSETTA-OSIRIS, VENUS EXPRESS) which have all successfully run. The architecture foresees three layers plus a boot loader (see Fig. 12) that resides in fixed memory. The approach is based on an RTOS and includes a dedicated Onboard Command Language (OCL), a compiler/interpreter system with a full C-like language set and macro-commands for functionalities specific to ASPIICS. OCL provides a flexible, safe, and easy to use implementation of in-flight reprogrammable procedures. OCL is inherited from various ESA/NASA instruments and satellites application SW.

Layer 1: Low Level S/W (HW dependent)

- Interface to the H/W with the next higher S/W level.
- Real-time operating system and driver software.
- Interfaces to both the RTOS and the driver S/W.

Layer 2: RTL and Middleware (HW independent)

- Command execution, also within several operational modes.
- Basic controlling functions, as so called RTL, e.g. for control of data processing, HK acquisition, etc. Also, control of file operations to and from image memory shall be allocated in the RTL.
- Autonomous, time- and event-driven, flexible, and safe instrument control system, On-board Command Language (OCL).

Layer 3: Application Layer (in OCL)

- High level application software, which is developed using the OCL functionalities, e.g. configurable management procedures for mode sequencing, data acquisition and processing sequencing, autonomous reactions on HK or data evaluation events, etc.

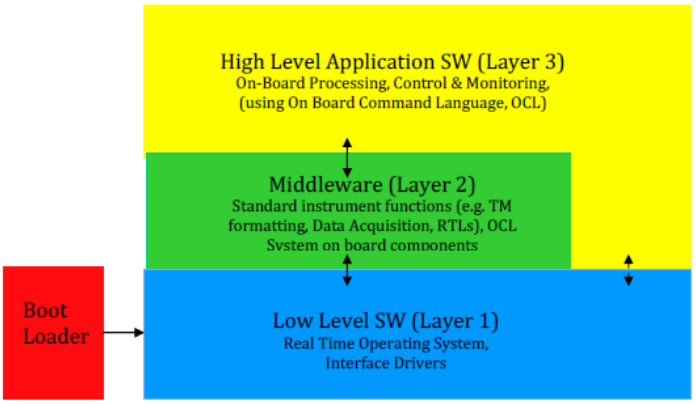

Figure 12. Software architecture

The proposed S/W design reflects the wide range of application driven requirements by means of built-in flexibility for:

- adaptability to different hardware interfaces,
- comprising RTOS to manage different prioritized tasks for both, control functions as well as data processing demands,
- providing means for accessing special function processors for on-line processing demands,
- autonomous control of instrument and data processing,
- provide modularity, e.g. for in-flight changes or updates, and
- failure tolerance to guarantee at least the main control and monitoring functions with uninterrupted performance.

13. Conclusions

In this paper the functional control electronics of the ASPIICS instrument mounted in the Coronagraph Control Box (CCB) have been presented as they have been defined at the Preliminary Design Review (PDR) status.

14. Acknowledges

This work has been funded by the European Space Agency ESA, the General Secretariat for Research and Technology (GSRT) and the Special Account for Research Grants (SARG) of the University of Athens, the Deutsches Zentrum für Luft-und Raumfahrt (DLR), and the Belgian Science Policy Office (BELSPO).

The authors would like to thank the ESA reviewers during the SRR and PDR processes for their valuable comments and remarks.

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